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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,573	01/18/2002	Tetsuo Yamada	Q66582	7082

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EXAMINER

DANIELS, ANTHONY J

ART UNIT	PAPER NUMBER
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2615

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/050,573

Applicant(s)

YAMADA ET AL.

Examiner

Anthony J. Daniels

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 4/13/2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Amendment***

1. The amendment, filed 4/13/2005, has been entered and made of record. Claims 1-12 are pending in the application.
2. Applicant's amendment to the title has overcome examiner's original objection.

### ***Claim Objections***

3. Claim 1 is objected to because of the following informalities: Unit, the last word of the claim should be plural. Appropriate correction is required.

### ***Response to Arguments***

4. Applicant's arguments, see Remarks, filed 4/13/2005, with respect to the rejection(s) of claim(s) 1-4 under Mizutani have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is being made (see rejections that follow).

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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5. Claims 1,2,5-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (US # 5,274,476).

As to claim 1, Lee teaches a charge read-out method (Figure 5), comprising the steps of: moving charges (Figure 5; Col. 5, Lines 52-54) into a plurality of charge transfer paths (Figure 5, VCCD regions) disposed on both sides along a row of a plurality of light receiving units (Figure 5, adjacent photodiodes; *{The examiner refers to a light receiving unit as photodiodes arranged adjacent (back-to-back to each other). In Figure 5, the photodiode labeled "PD64" and the photodiode directly to the left together are considered a unit.}*), arranged linearly (Figure 5, units arranged linearly in the row direction), the charges being generated and stored in the plurality of light receiving units having received light (Col. 5, Lines 52-54); and transferring and outputting the moved charges along the light receiving paths disposed on both sides of the plurality of light receiving unit (Figure 5, Col. 6, Lines 3-11).

As to claim 2, Lee teaches a solid-state imaging device (Figure 5, CCD image sensor), comprising: a plurality of light receiving units (Figure 5, adjacent photodiodes; *{The examiner refers to a light receiving unit as photodiodes arranged adjacent (back-to-back to each other). In Figure 5, the photodiode labeled "PD64" and the photodiode directly to the left together are considered a unit.}*), arranged linearly (Figure 5, units arranged linearly in the row direction) for receiving light to generate and store charges (Col. 5, Lines 52-54); a plurality of charge transfer paths (Figure 5, VCCD regions) disposed on both sides of said plurality of light receiving units (Figure 5) for receiving the charges exiting from said plurality of light receiving units and for transferring and outputting the received charges (Col. 6, Lines 3-11); a controller for moving the charges stored in said plurality of light receiving units into said plurality of charge transfer paths,

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and for transferring and outputting the charges moved into said plurality of charge transfer paths disposed on both sides of said plurality of light receiving units (Col. 6, Lines 47-64; *{It is inherent that the clock signals are generated from some circuitry in connection with the CCD image sensor.}*).

As to claim 5, Lee teaches the charge read-out method according to claim 1, wherein each of the plurality of light receiving units is connected to a light receiving path on at least two sides to permit the charges to exit from both sides of the light receiving unit (Figure 5, arrows pointing toward VCCD regions; Figure 6; Col. 6, Lines 47-64).

As to claim 6, Lee teaches the solid-state imaging device according to claim 2, wherein each of the plurality of light receiving units is directly connected to at least two transmission gates (Figure 6, transfer gates "TG1" - "TG4"), and wherein each of the two transmission gates facilitates transmission of the charge from its respective light receiving unit to a charge transfer path (Col. 7, Lines 59-68; Col. 8, Lines 1-13).

As to claim 7, Lee teaches the solid-state imaging device according to claim 2, wherein the charges from a light receiving unit of the plurality of light receiving units exit the light receiving unit on both sides and are transmitted to a respective charge transfer path from the plurality of charge transfer paths (Figure 5, Figure 6).

### ***Claim Rejections - 35 USC § 103***

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

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evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 3,4,8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato (US # 6,337,713) in view of Burke et al. (US # 6,331,873).

As to claim 3, Sato teaches a solid-state imaging device (Figure 2, CCD image sensor "104") comprising: a plurality of light receiving units (Figure 2, image pixel sections "A" - "D") arranged linearly (Figure 2, sections are arranged linearly in the vertical and horizontal directions) for receiving light to generate and store charges (Figure 2, CCD elements "1-100"; Col. 6, Lines 48-59); a plurality of charge transfer paths (Figure 2, horizontal CCD transfer paths "128A" - "128D") disposed on both sides of said plurality of light receiving units (Figure 2) for receiving the charges exiting from said plurality of light receiving units and for transferring and outputting the received charges (Col. 6, Lines 60-67); a controller for moving the charges stored in said plurality of light receiving units into said plurality of charge transfer paths, and for transferring and outputting the charges moved into said plurality of charge paths disposed on both sides of said plurality of light receiving units (Figure 2, CCD driver "106"), wherein each of said plurality of light receiving units includes a plurality of segments so that the charges stored

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in said plurality of light receiving units are moved said plurality of charge transfer paths (Figure 2, in image pixel sections “A” – “D”, each contains segments 1,2,11,12). The claim differs from Sato in that it further requires that the plurality of segments be separated by a potential barrier.

In the same field of endeavor, Burke et al. teaches a blooming control structure using a potential barrier to deflect photo-generated electrons toward channels (Figure 11E, Col. 7, Lines 28-67). In light of the teaching of Burke et al., it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the blooming control structure of Burke et al. to separate the image pixel sections of Sato, because an artisan of ordinary skill in the art would recognize that this effectively prevents a decrease in charge accumulation and a reduction in quantum efficiency due to the interaction of charges of separate pixel sites (i.e. blooming) (see Burke et al., Col. 8, Lines 10-18). *The combination of Burke et al. with Sato places blooming control structures between all adjacent pixel sites including the pixel cite labeled 1,2,11,12 in Sato.*

As to claim 4, Sato teaches the solid-state imaging device according to claim 3, wherein the plurality of segments are four segments obtained by separating each of said plurality of light receiving units with a cruciform potential barrier (see Sato, barrier locations at 1,2,11,12 form a cruciform barrier).

As to claim 8, Sato, as modified by Burke et al., teaches the solid-state imaging device according to claim 3, wherein the barrier comprises: a first conductive impurity layer (see Burke et al., Figure 11E, p+ “48”) and a second conductive impurity layer (see Burke et al., Figure 11E, n- “40” and insulating layers) selectively formed on top of the first conductive impurity layer (see Burke et al., Figure 11E), the second conductive impurity layer has a surface covered with a

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first conductive high density layer in a light receiving unit from the plurality of light receiving units (see Burke et al., Figure 11E, p+ “84”), and wherein the second conductive impurity layer or the first conductive impurity layer is of relative low density (see Burke et al., Figure 11E, second layer (n-)).

As to claim 9, Sato, as modified by Burke et al., teaches the solid-state imaging device according to claim 3, wherein the barrier comprises a PNP structure (see Burke et al., Figure 11E, p+ “48”, n- “40”, p+ “84”), formed on a p-substrate (see Burke et al., Figure 11E, p-substrate “42”).

As to claim 10, Sato, as modified by Burke et al., teaches the solid-state imaging device according to claim 3, wherein the barrier is provided without impeding photoelectric conversion of its respective light receiving unit (see Burke et al., Col. 7, Lines 28-32; *{If photo-generated electrons exist, then the conversion has not been impeded.}*).

As to claim 11, Sato, as modified by Burke et al., teaches the solid-state imaging device according to claim 3, wherein the segments separated by the potential barrier are triangularly shaped (see Sato; *{Looking at the image sensor from a 45 degree angle shows two sides of a triangle defined by the line between pixel sites 1 and 11 and the line between pixel sites 11 and 12.}*).

As to claim 12, Sato teaches the solid-state imaging device according to claim 3, wherein the potential barrier diagonally divides a light receiving unit from the plurality of light receiving units into segments (see Sato; *{Looking at the sensor from a 45 degree angle shows a diagonal line defined by the line between 1 and 11 and 2 and 12.}*).




*Conclusion*

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony J. Daniels whose telephone number is (571) 272-7362. The examiner can normally be reached on 8:00 A.M. - 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AD  
10/4/2005

  
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SUPERVISORY PATENT  
EXAMINER